4610

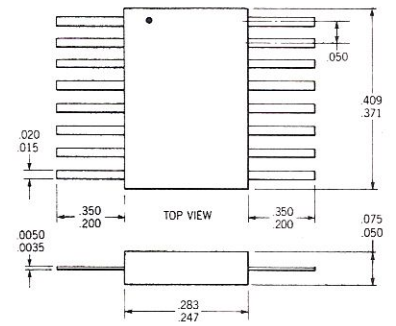
DUAL TWO-VARIABLE FUNCTION GENERATOR

TTL MICROMATRIX™ ARRAY CIRCUIT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION—The 4610 is a Dual Two-Variable Function Generator useful for non-arithmetic operations and variable decision making control in central processor units. Each circuit, controlled by a common 4-bit word, can select one of 16 possible Boolean functions performed on the two variable inputs. An alternate input select configuration increases circuit flexibility and allows simultaneous generation of two separate output functions from a single pair of variables. **The circuit is produced with two layer metal interconnection using the Fairchild 4600 TTL Micromatrix™ Array.**

FLAT PACKAGE



FEATURES

- **EXPANDABLE IN GROUPS OF 2 BITS**
- **MEMBER OF 4600 MICROMATRIX ARRAY FAMILY**
- **CCSL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16-PIN FLAT PACK**
- **TWO LAYER METAL INTERCONNECTIONS**
- **SIMULTANEOUS FUNCTIONS OF 1 PAIR OF VARIABLES**

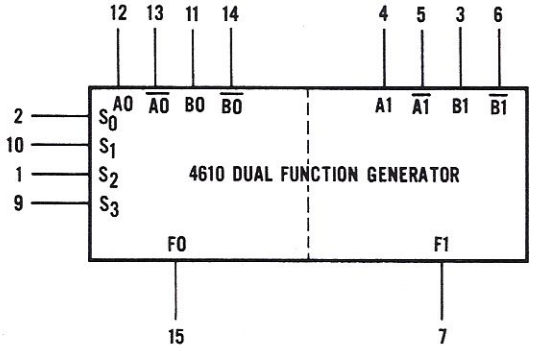
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs (Output high)	Gnd to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output (Output low)	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify A3L46105XX for Flat package, where 51X is for −55°C to +125°C (Case) temperature range or 59X for the 0°C to +75°C (Case) temperature range.

FIG. 1 — 4610 DUAL TWO-VARIABLE FUNCTION GENERATOR



Pin 16 = Vcc
Pin 8 = Gnd

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FAIRCHILD SEMICONDUCTOR
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ELECTRICAL CHARACTERISTICS ($T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 9.92\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		.75	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{12}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

ELECTRICAL CHARACTERISTICS ($T_C = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 11.3\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.08	−1.60		−1.60	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current					60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{12}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

FUNCTION GENERATOR DESCRIPTION

A detailed logic representation of the common control (S_0, S_1, S_2, S_3) and one of the two output function blocks is shown in Figure 2. The Truth Table implemented by the function generator shows the functions of input variables A and B with the 16 possible combinations of S_0, S_1, S_2, and S_3 (refer to Table 1). Note that any desired output function may be chosen active level high or active level low.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH

S_0	S_1	S_2	S_3	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$A + B$	$\overline{A} \cdot \overline{B}$
L	H	L	L	$A + \overline{B}$	$\overline{A} \cdot B$
H	L	L	L	$\overline{A} + B$	$A \cdot \overline{B}$
H	H	L	L	$\overline{A} + \overline{B}$	$A \cdot B$
L	L	L	H	$\overline{A} \cdot \overline{B}$	$A + B$
L	H	L	H	$\overline{A} \cdot B$	$A + \overline{B}$
H	L	L	H	$A \cdot \overline{B}$	$\overline{A} + B$
H	H	L	H	$A \cdot B$	$\overline{A} + \overline{B}$
L	L	H	L	$A \oplus B$	$A \oplus \overline{B}$
L	H	H	L	$A \oplus \overline{B}$	$A \oplus B$
H	L	H	L	1	0
H	H	H	L	0	1
L	L	H	H	A	$\overline{A}$
L	H	H	H	B	$\overline{B}$
H	L	H	H	$\overline{A}$	A
H	H	H	H	$\overline{B}$	B

TABLE 1

DETAILED LOGIC DIAGRAM

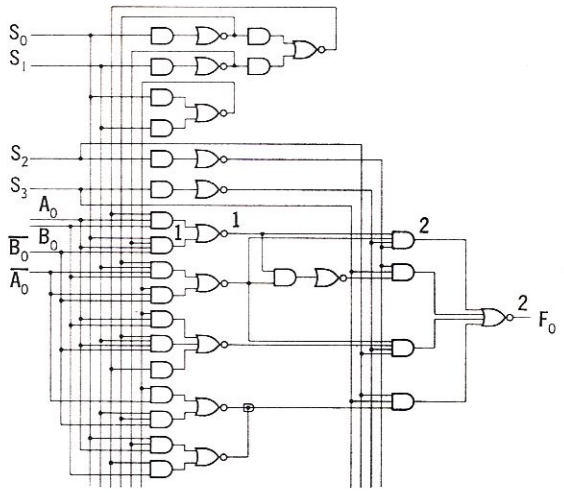


FIG. 2

Circuit flexibility can be increased by using S_2, S_3, A and B inputs as controls and S_0, S_1 as the input variables. In this mode of operation two separate output functions are performed simultaneously on a single pair of variables S_0 and S_1. Refer to Table 2 below for complete truth table.

For example, if it is desired to obtain the active high functions $\overline{S}_0 \cdot S_1$ and $S_0 \cdot \overline{S}_1$ simultaneously, S_2, S_3 are set low, A_0 low, B_0 high, A_1 high, and B_1 low. The function $\overline{S}_0 \cdot S_1$ will appear at the F_0 output; likewise function $S_0 \cdot \overline{S}_1$ will appear at the F_1 output.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH WHERE A, B, S_2, S_3 ARE USED AS CONTROL INPUTS AND S_0, S_1 ARE INPUT VARIABLES ON WHICH THE FUNCTIONS ARE PERFORMED.

S_2	S_3	A	B	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$S_0 + S_1$	$\overline{S}_0 \cdot \overline{S}_1$
L	L	L	H	$S_0 + \overline{S}_1$	$\overline{S}_0 \cdot S_1$
L	L	H	L	$\overline{S}_0 + S_1$	$S_0 \cdot \overline{S}_1$
L	L	H	H	$\overline{S}_0 + \overline{S}_1$	$S_0 \cdot S_1$
L	H	L	L	$\overline{S}_0 \cdot \overline{S}_1$	$S_0 + S_1$
L	H	L	H	$\overline{S}_0 \cdot S_1$	$S_0 + \overline{S}_1$
L	H	H	L	$S_0 \cdot \overline{S}_1$	$\overline{S}_0 + S_1$
L	H	H	H	$S_0 \cdot S_1$	$\overline{S}_0 + \overline{S}_1$
H	L	L	L	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	L	L	H	$\overline{S}_1$	S_1
H	L	H	L	$\overline{S}_1$	S_1
H	L	H	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	L	L	S_0	$\overline{S}_0$
H	H	L	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	H	L	$S_0 \oplus \overline{S}_1$	$S_0 \oplus S_1$
H	H	H	H	$\overline{S}_0$	S_0

TABLE 2

Note that by varying control lines S_2, S_3, A and B that any pair of S_0 and S_1 min terms, max terms, or symmetric function can be generated.

LOADING RULES

Input Loading Rules (Fan-in)

1. I_F is defined as one low level unit load. The multipliers to determine low level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
S_2, S_3	5
A_0, A_1, B_0, B_1 $\overline{B_0}$, $\overline{B_1}$	4
$\overline{A_0}$, $\overline{A_1}$	3

2. I_R is defined as one unit high level load. The multipliers to determine high level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
A_0, A_1, S_2, S_3	5
$\overline{B_0}$, $\overline{B_1}$, B_0, B_1	4
$\overline{A_0}$, $\overline{A_1}$	3

FAN OUT

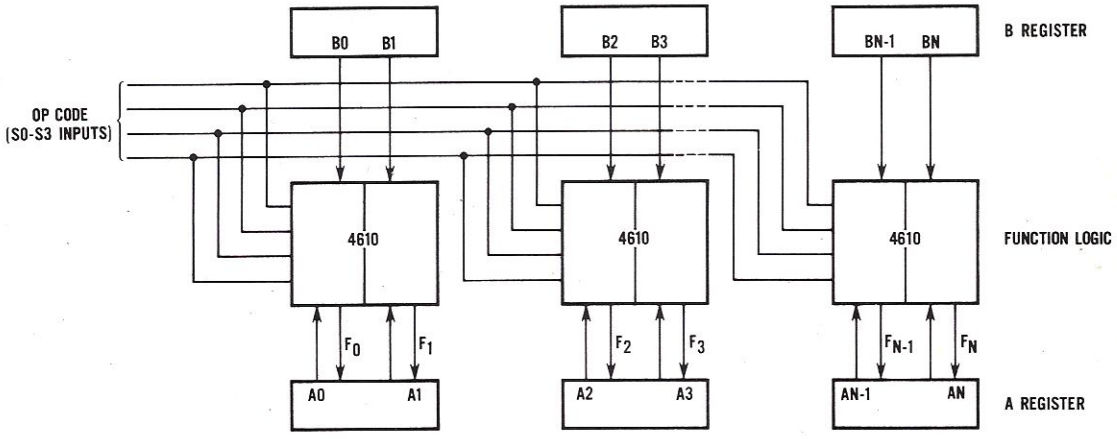
	LEVEL	
OUTPUT	HIGH	LOW
F_0	20	8
F_1	20	8

APPLICATIONS

A Typical Processor Application is the transfer and logical operation control between two registers (A and B). The function generators are controlled by a 4-bit operation code field, S_0, S_1, S_2, and S_3. The operation code repertoire includes the 16 operations listed below.

AND $\overline{A}$ and $\overline{B}$ to A	OR A and B to A
AND $\overline{A}$ and B to A	OR A and $\overline{B}$ to A
AND A and $\overline{B}$ to A	OR $\overline{A}$ and B to A
AND A and B to A	OR $\overline{A}$ and $\overline{B}$ to A
Exclusive OR A and $\overline{B}$ to A	Complement A
Exclusive OR A and B to A	Transfer $\overline{B}$ to A
Reset A	No Operation
Set A	Transfer B to A

FIG. 3



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